REMARKS

This is intended as a full and complete response to the Office Action dated January 25, 2005, having a shortened statutory period for response set to expire on April 25, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-6, 12-17, 19-24 and 29-38 are pending in the application and remain pending following entry of this response.

Claim Rejections - 35 U.S.C. § 103

Claims 1-6, 12-14, 19-24, 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin, November 1993, US (hereinafter "IBM") as applied to claim 1, 12, and 19 and further in view of *Parks* (US. 6,594,736). Applicants respectfully traverse this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143.

The present rejection fails to establish at least the third criteria. In other words, Applicants submit the references, alone or in combination, do not teach, show, or suggest, executing, by a processor, a cache purge instruction that configures the processor to send a cache line to at least one of a plurality of processors.

IBM states that "the coherence unit tracks all nodes having copies of local addresses so it knows to whom it must send purges." Thus, *IBM* discloses a *coherency unit* (*See IBM*, Figure 1), and not a processor, sends purge information to each of the nodes. No cache purge instruction, executed by a processor, is taught or suggested in *IBM*.

While *Parks* describes migrating a cache line with write access from one processor to another, *Parks* states that migrating a cache line may require "*multiple read transactions along with one or more cache coherency operations and their accompanying replies.*" Thus, in *Parks*, migration is performed with multiple read transactions and cache coherency operations. In contrast, the present claims recite executing a single cache purge instruction which sends the cache line to at least one of a plurality of processors.

Therefore, *Parks* or *IBM*, either alone or in combination, do not teach, show, or suggest a cache purge instruction executed by a processor, as claimed. Accordingly, Applicants submit claims 1, 12, and 19, as well as their dependents, are patentable over *IBM* and further in view of *Parks*. Withdrawal of the rejection is respectfully requested.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, *Parks*, and further in view of *AAPA (assumed to stand for "applicants' admitted prior art")*. The Examiner takes the position that *IBM* and *Parks* teach the claimed elements but for marking a state of updated cache lines as *temporarily invalid*, which the Examiner states is taught by *AAPA*. For reasons discussed above, Applicants submit that *IBM*, alone or in combination with *Parks*, fails to teach the claimed cache purge instruction executed by a processor.

Further, Applicants submit that marking a state of cache lines as *temporarily invalid* is not admitted prior art. While Applicants state that a cache directory 200 may be configured as is known in the art (paragraph 30, lines 1-2), there is no statement that marking an entry as *temporarily invalid* is known in the art.

Therefore, Applicants submit that claim 30 is patentable over *IBM*, *Parks*, and further in view of *AAPA*. Withdrawal of the rejection is respectfully requested.

Claims 15-16 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, *Parks*, and further in view of *Yates*.

The Examiner takes the position that *IBM*, when combined with *Parks*, teaches the claimed elements, but for the purge instruction referencing at least five fields, which the Examiner states is taught by *Yates*. For reasons discussed above, Applicants submit that *IBM*, alone or in combination with *Parks*, fails to teach a cache purge instruction executed by a processor.

Therefore, Applicants submit that claims 15-16 and 34 are patentable over *IBM*, *Parks*, and further in view of *Yates*. Withdrawal of the rejection is respectfully requested.

Claims 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, *Parks*, and further in view of *Liu* (US 5,210,848).

The Examiner takes the position that *IBM*, when combined with *Parks*, teaches the claimed elements, but for updating only one cache at a designated processor and marking a state of the updated cache line as exclusive at the designated processor, which the Examiner states is taught by *Liu*. For reasons discussed above, Applicants submit that IBM, alone or in combination with *Parks*, fails to teach the claimed a cache purge instruction executed by a processor.

Therefore, Applicants submit that claims 31-33, and 36-38 are patentable over *IBM*, *Parks*, and further in view of *Liu*. Withdrawal of the rejection is respectfully requested.

Applicants note that claim 17 is indicated as rejected on the Office Action Summary, but is not explicitly discussed in the Office Action. Applicants request clarification of the status of this claim.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

Randol W. Read
Registration No. 43,876
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants